General Purpose Transistors

PNP Silicon

Features

• These are Pb-Free Devices

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector - Emitter Voltage	V_{CEO}	-40	Vdc
Collector - Base Voltage	V_{CBO}	-40	Vdc
Emitter – Base Voltage	V_{EBO}	-5.0	Vdc
Collector Current – Continuous	I _C	-200	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board (Note 1) @ T _A = 25°C Derate above 25°C	P _D	225 1.8	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate, (Note 2) @ T _A = 25°C Derate above 25°C	P _D	300 2.4	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T _J , T _{stg}	-55 to +150	°C

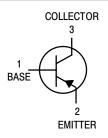
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. FR-5 = $1.0 \times 0.75 \times 0.062$ in.
- 2. Alumina = $0.4 \times 0.3 \times 0.024$ in. 99.5% alumina.



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SOT-23 CASE 318 STYLE 6

MARKING DIAGRAM



396 = Specific Device Code

M = Date Code*= Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

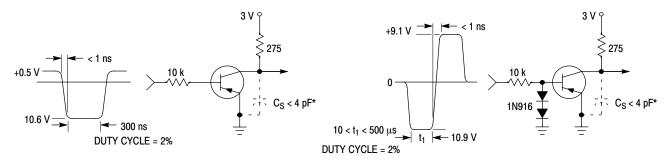
Device	Package	Shipping [†]
NSCT3906LT1G	SOT-23 (Pb-Free)	3,000 Tape & Reel
NSCT3906LT3G	SOT-23 (Pb-Free)	10,000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

$\textbf{ELECTRICAL CHARACTERISTICS} \ (T_A = 25^{\circ}C \ unless \ otherwise \ noted)$

Charac	teristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS						
Collector – Emitter Breakdown Voltage $(I_C = -1.0 \text{ mAdc}, I_B = 0)$		V _{(BR)CEO}	-40	_	Vdc	
Collector – Base Breakdown Voltage ($I_C = -10 \mu Adc, I_E = 0$)	V _{(BR)CBO}	-40	_	Vdc		
Emitter – Base Breakdown Voltage ($I_E = -10 \mu Adc, I_C = 0$)		V _{(BR)EBO}	-5.0	-	Vdc	
Base Cutoff Current ($V_{CE} = -30 \text{ Vdc}$, $V_{EB} = -3.0 \text{ Vdc}$)		I _{BL}	-	-50	nAdc	
Collector Cutoff Current (V _{CE} = -30 Vdc, V _{EB} = -3.0 Vdc)	I _{CEX}	-	-50	nAdc		
ON CHARACTERISTICS (Note 3)						
DC Current Gain		H _{FE}	60 80 100 60 30	- 300 - -	-	
Collector – Emitter Saturation Voltage ($I_C = -10 \text{ mAdc}$, $I_B = -1.0 \text{ mAdc}$) ($I_C = -50 \text{ mAdc}$, $I_B = -5.0 \text{ mAdc}$)		V _{CE(sat)}	_ _	-0.25 -0.4	Vdc	
Base – Emitter Saturation Voltage ($I_C = -10$ mAdc, $I_B = -1.0$ mAdc) ($I_C = -50$ mAdc, $I_B = -5.0$ mAdc)		V _{BE(sat)}	-0.65 -	-0.85 -0.95	Vdc	
SMALL-SIGNAL CHARACTERISTICS						
Current – Gain – Bandwidth Product ($I_C = -10 \text{ mAdc}, V_{CE} = -20 \text{ Vdc}, 1$	= 100 MHz)	f _T	250	_	MHz	
Output Capacitance $(V_{CB} = -5.0 \text{ Vdc}, I_E = 0, f = 1.0 \text{ M})$	Hz)	C _{obo}	-	4.5	pF	
Input Capacitance ($V_{EB} = -0.5 \text{ Vdc}$, $I_C = 0$, $f = 1.0 \text{ M}$	Hz)	C _{ibo}	_	10	pF	
Input Impedance ($I_C = -1.0 \text{ mAdc}$, $V_{CE} = -10 \text{ Vdc}$,	f = 1.0 kHz)	h _{ie}	2.0	12	kΩ	
Voltage Feedback Ratio ($I_C = -1.0 \text{ mAdc}, V_{CE} = -10 \text{ Vdc},$	h _{re}	0.1	10	X 10 ⁻⁴		
Small – Signal Current Gain ($I_C = -1.0 \text{ mAdc}, V_{CE} = -10 \text{ Vdc},$	h _{fe}	100	400	-		
Output Admittance ($I_C = -1.0 \text{ mAdc}$, $V_{CE} = -10 \text{ Vdc}$,	h _{oe}	3.0	60	μmhos		
Noise Figure (I _C = $-100 \mu Adc$, V _{CE} = $-5.0 Vdc$,	NF	-	4.0	dB		
SWITCHING CHARACTERISTICS						
Delay Time	$(V_{CC} = -3.0 \text{ Vdc}, V_{BE} = 0.5 \text{ Vdc},$	t _d	_	35	ne	
Rise Time	$I_C = -10 \text{ mAdc}, I_{B1} = -1.0 \text{ mAdc})$	t _r	_	35	ns	
Storage Time	$(V_{CC} = -3.0 \text{ Vdc}, I_{C} = -10 \text{ mAdc},$	t _s	_	225	ns	
Fall Time	$I_{B1} = I_{B2} = -1.0 \text{ mAdc}$	t _f	_	75		

^{3.} Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.



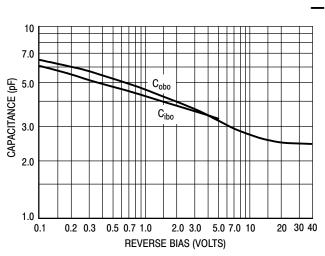
* Total shunt capacitance of test jig and connectors

Figure 1. Delay and Rise Time Equivalent Test Circuit

Figure 2. Storage and Fall Time Equivalent Test Circuit

TYPICAL TRANSIENT CHARACTERISTICS

- T_J = 25°C



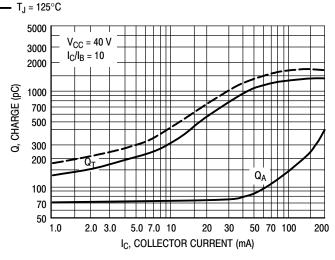
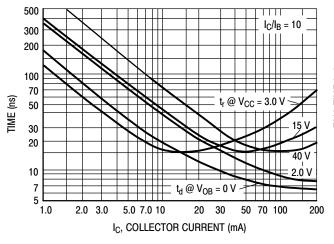


Figure 3. Capacitance

Figure 4. Charge Data



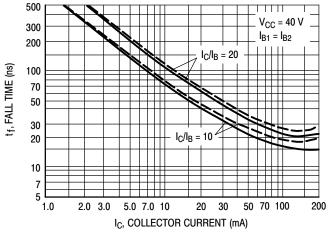
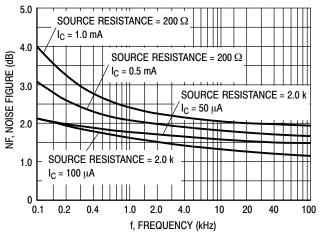


Figure 5. Turn-On Time

Figure 6. Fall Time

TYPICAL AUDIO SMALL-SIGNAL CHARACTERISTICS NOISE FIGURE VARIATIONS

 $(V_{CE} = -5.0 \text{ Vdc}, T_A = 25^{\circ}\text{C}, Bandwidth = 1.0 \text{ Hz})$



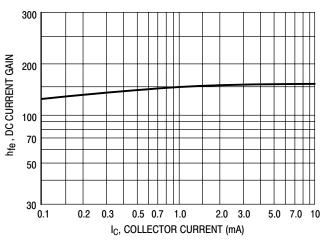
f = 1.0 kHz 10 NF, NOISE FIGURE (dB) 8 6 4 $I_{C} = 50 \, \mu A$ $I_C = 100 \mu A$ 2 0.1 0.2 2.0 4.0 40 0.4 1.0 100 R_a, SOURCE RESISTANCE (k OHMS)

Figure 7.

Figure 8.

h PARAMETERS

 $(V_{CE} = -10 \text{ Vdc}, f = 1.0 \text{ kHz}, T_A = 25^{\circ}\text{C})$



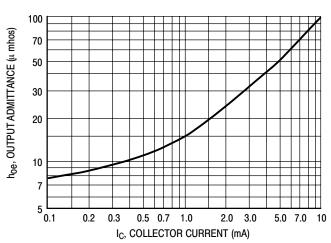
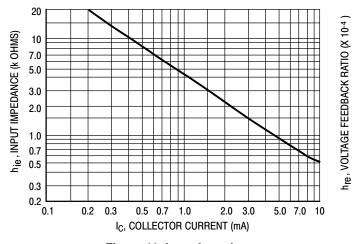


Figure 9. Current Gain

Figure 10. Output Admittance



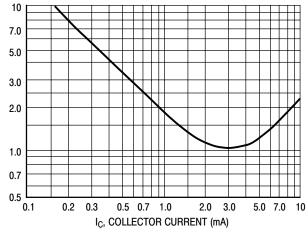


Figure 11. Input Impedance

Figure 12. Voltage Feedback Ratio

TYPICAL STATIC CHARACTERISTICS

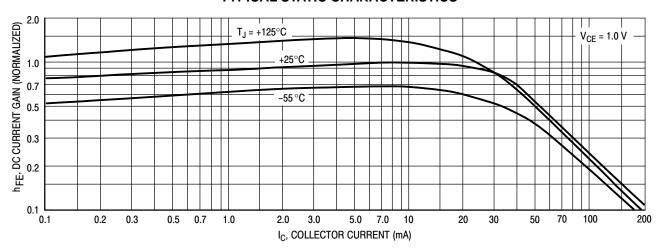


Figure 13. DC Current Gain

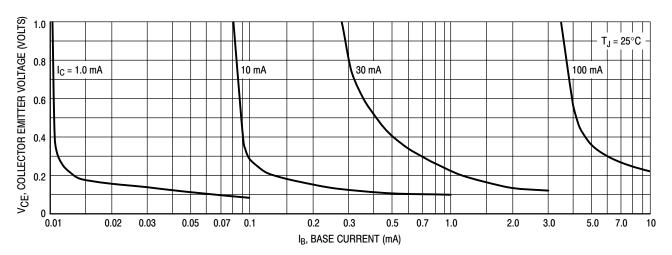


Figure 14. Collector Saturation Region

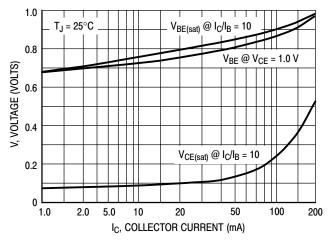


Figure 15. "ON" Voltages

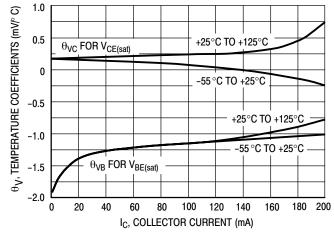
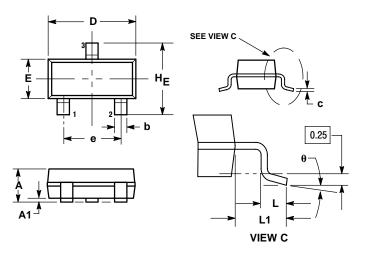


Figure 16. Temperature Coefficients

PACKAGE DIMENSIONS

SOT-23 (TO-236) CASE 318-08 ISSUE AN



NOTES:

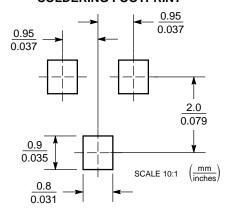
- DIMENSIONING AND TOLERANCING PER ANSI
 V14 5M 1082
- Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.
- MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
- 4. 318-01 THRU -07 AND -09 OBSOLETE, NEW STANDARD 318-08.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
С	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
е	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 6:

- PIN 1. BASE 2. EMITTER
 - EMITTER
 COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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